Electronic Version
Stylesheet Version v1.1.1

Claims

[c1] What is claimed is:

[c2] 1. A sensing circuit for sensing the logic data stored in a memory cell, the memory cell being electrically connected to a bit line, the sensing circuit comprising:
a first pre-charging module, electrically connected to the bit line, for pre-charging the bit line;
a selecting module, electrically connected to the bit line and a first data line, for transmitting signals of the bit line to the first data line according to a first controlling signal and isolating the capacitance of the bit line and the first data line;
a second pre-charging module, electrically connected to the first data line, for pre-charging the first data line;
a first voltage keeping module, electrically connected to the first data line, for maintaining the signal on the first data line at a high voltage level when a logic value "1" is stored in the memory cell;
an isolating module, electrically connected between the first data line and a second data line, for transmitting signals from the first data line to the second data line according to a second controlling signal and isolating

the capacitance of the first data line and the second data line; and

a third pre-charging module, electrically connected to the second data line, for pre-charging the second data line.

[c3] 2. The sensing circuit of claim 1 wherein the first voltage keeping module comprises:

a PMOS transistor, the source being electrically connected to a power supply voltage, the drain being electrically connected to the first data line; and

a NAND logic gate, comprising two input ends and one output end, the two input ends being electrically connected to the first data line, the output end being electrically connected to the gate of the PMOS transistor.

[c4] 3. The sensing circuit of claim 1 further comprising a second voltage keeping module, electrically connected to the second data line, for maintaining the signal on the second data line at a high voltage level when a logic value "1" is stored in the memory cell.

[c5] 4. The sensing circuit of claim 3 wherein the second voltage keeping module comprises:

a PMOS transistor, the source being electrically connected to a power supply voltage, the drain being electrically connected to the second data line; and

a NAND logic gate, comprising two input ends and one output end, the two input ends being electrically connected to the second data line, the output end being electrically connected to the gate of the PMOS transistor.

[c6] 5. The sensing circuit of claim 4 further comprising a waveform reshaping module, electrically connected to the second data line, for sensing the signals of the second data line in order to generate an output signal on an output signal line.

[c7] 6. The sensing circuit of claim 5 wherein the waveform reshaping module comprises:
a first inverter, comprising an input end and an output end, the input end being electrically connected to the second data line;
a second inverter, comprising an input end and an output end, the input end being electrically connected to the output signal line;
a first NMOS transistor, the drain being electrically connected to the second data line, the gate being electrically connected to the output end of the second inverter; and
a second NMOS transistor, the drain being electrically connected to the output signal line, the gate being electrically connected to the output end of the first inverter.

[c8] 7. The sensing circuit of claim 6 wherein the waveform

reshaping module further comprises:
a third NMOS transistor, the drain being electrically connected to the source of the first NMOS transistor, the gate being electrically connected to a third controlling signal, the source being electrically connected to ground; and
a fourth NMOS transistor, the drain being electrically connected to the source of the second NMOS transistor, the gate being electrically connected to the third controlling signal, the source being electrically connected to ground.

[c9] 8. The sensing circuit of claim 5 wherein the waveform reshaping module further comprises a fourth pre-charging module, electrically connected to the output signal line, for pre-charging the output signal line.

[c10] 9. The sensing circuit of claim 8 wherein the fourth pre-charging module is a PMOS transistor, the drain being electrically connected to the output signal line, the gate being electrically connected to the second controlling signal, and the source being electrically connected to the power supply voltage.

[c11] 10.The sensing circuit of claim 5 wherein the waveform reshaping module further comprises a PMOS transistor, the drain being electrically connected to the output sig-

nal line, the gate being electrically connected to the output end of the NAND logic gate of the second voltage keeping module, the source being electrically connected to the power supply voltage.

[c12] 11.The sensing circuit of claim 1 wherein the first pre-charging module is a NMOS transistor, the drain being electrically connected to the bit line, the gate being electrically connected to the inverted signal of the first controlling signal, the source being electrically connected to ground.

[c13] 12.The sensing circuit of claim 1 wherein the selecting module is a NMOS transistor, the drain being electrically connected to the first data line, the gate being electrically connected to the first controlling signal, the source being electrically connected to the bit line.

[c14] 13. The sensing circuit of claim 1 wherein the second pre-charging module is a PMOS transistor, the drain being electrically connected to the first data line, the gate being electrically connected to the second controlling signal, the source being electrically connected to a power supply voltage.

[c15] 14.The sensing circuit of claim 1 wherein the isolating module is a NMOS transistor, the drain being electrically

connected to the second data line, the gate being electrically connected to the second controlling signal, the source being electrically connected to the first data line.

[c16] 15.The sensing circuit of claim 1 wherein the third precharging module is a PMOS transistor, the drain being electrically connected to the second data line, the gate being electrically connected to the second controlling signal, the source being electrically connected to a power supply voltage.